1 Software Pipelining

for(i = 0; i < n; i++) {
    X[i+1] = X[i] * 2
    Y[i+1] = X[i+1] + Y[i]
}

1: LD R2 *(R0++)
2: MUL R3, R2, $2
3: ST *(R0), R3
4: LD R4, *(R0)
5: LD R5, *(R1++)
6: ADD R6, R4, R5
7: ST *(R1) R6

For this problem, assume that ADD/MUL takes 2 clocks, while LD/ST takes 1 clock. The machine has two MEM units that can execute a LD and ST, and two ALU units. The machine can auto-increment address registers.

Given the above instructions corresponding to the snippet of code, draw the data dependence graph.
What is the lower bound on the initiation interval (ignoring resource constraints)?

4 due to the cycle length of 4 and iteration difference of 1.
2 Dependency Analysis

for(i = 1; i < n; i++) {
    for(j = i; j < 2 * i; j++) {
    }
}

Draw the iteration space for this loop.

Solution:

What are all the candidates for data dependencies in this loop? A data dependency is something of the form “read/write $A[i]$, read/write $B[j]$”.

- read $A[i-1, j]$, write $A[i, 2*j]$
- write $A[i, 2*j]$, read $A[i-1, j]$ (across iterations)
3 Software Pipelining with Resource Constraints

Consider the following dependence graph for a single iteration of a loop, with resource constraints:

1. What is the bound on the initiation interval $T$ according to the precedence and resource constraints for this program?
   
   4 due to data dependence in cycle $\text{Max} \ (\text{cycle length/ iteration diff}) = 4/1 = 4$
   
   4 due to resource constraints as well.

2. What is the minimum initiation interval? Show a modulo reservation table for an optimal software pipelined schedule. Also show the code and schedule for an iteration in the source loop.

   The minimum initiation interval is 4. Modulo reservation table:

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<tr>
<td>A</td>
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<td>D</td>
<td>D</td>
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   Single iteration: A, nop, nop, B, nop, nop, nop, nop, nop, C, D, nop, E